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2) Limit your search by using search operators and field codes, if desired.
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parity<and>decoding<and>recording

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Note: This function returns plural and suffixed forms of the keyword(s).

Search operators: <and> <or> <not> <in> More

Field codes: au (author), ti (title), ab (abstract), jn (publication name), de (index term) More

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parity<and>decoding<and>magnetic<and>recording

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DISCLOSURE TITLE: Correction Methods for Errors in Partial Response Channels. March 1970.

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DISCLOSURE TEXT:

7p. The methods are for correcting a wide class of errors in partial response channel, Ref. 1, or any linear channel whose response can be described as the outcome of a digital modulation or correlative level coding schemes, Refs. 2 and 3. The methods to be described find application in magnetic recording as well as in data communication since a magnetic recording channel can be regarded as a partial response channel.

- A system of detecting errors in a digital modulation system, equivalent to a correlative level coding or partial response channel, is shown in drawing 1. D is the delay operator. G(D) is a polynomial of D and takes a special form in each application. The following are some examples of digital modulation or a partial response channel system.

- In data Transmission for a duobinary system G(D) = 1 + D and for a partial response channel, Class IV, Ref. 1, or a modified duobinary system G(D) = 1 - D2. In magnetic recording for a two-level Saturation Recording with NRZI G(D) = 1 + D and for an interleaved NRZI with Channel Shaping G(D) = 1 - D2.

- The main features of these methods are as follows. Almost all single errors can be corrected instantly or with a finite delay. More than half of double errors are correctable. Some multiple errors are also correctable. The correction algorithm and circuits are of a general form, i.e., error correction circuits can be arranged for any G(D) and for any m, the number of signal levels. Use of a parity check code allows correction of all correctable errors with a maximum delay equal to the span of parity bit checks. Error Correction in Partial Response Channels.

- Consider the magnetic saturation recording with NRZI. In this case, m = 2 and G(D) = 1 - D. The channel output [x(k)] corresponds to the read head output, drawing 1. In the absence of intersymbol interference and noise, the level slicer output ["c(k)] takes one of three possible levels identified as 2, 0, or -2. Thus the threshold of the level slicer is set at 1 and -1. An error occurs when the channel output [x(k)] exceeds and falls in a false decision region. However, in practice, almost all erroneous received signals, x(k)'s which cross the thresholds in the above example, still lie in the neighborhood of the corresponding threshold. A modified decision rule with the level slicer as follows:

See original p1725. where delta < 1 is a predetermined constant,

drawing 2.

- The output of Digital Demodulator [b(k)] given by b(k) = b(k-1) + c(k) takes new levels such as 1, 3 and i1 besides 2 and 0. The levels 3 and -1 are outside of the legitimate levels 2 and 0.
- In connection with the principle of error correction, the location "k" of any level slicer output with c(k) = 1 or -1 is identified and stored temporarily. Also, the polarity of error is determined when a Digital Demodulator output b(k), = 3 or i1 (k'>/- k) is received.
- The decision rule is similar to the null zone detection method, e.g., Ref. 4. The correction algorithm in the system of drawing 1 offers significant advantages in the following aspects. There is no complicated logic to recognize an unacceptable sequence other than the Digital Demodulator. Thus, the method of correction is not only simpler, but also takes a general form which is immediately generalizable to cases with different type of partial response channels and an arbitrary number of signal levels. The method is subject to no change when block **coding** with a single **parity** digit is adopted in the information sequence. The system retains its full capacity of detecting all unacceptable sequences due to uncorrectable errors.

The following examples illustrate the method. Example 1 m = 2, G(D) = 1-D, magnetic **recording** with NRZI

See original p1726.

- The structure of the receiver has the following aspects. The Level Slicer output [c(k)] takes five different levels, i.e., 3, 2, 1, 0 and -1. The Digital Demodulator has the form

See original p1726. Similarly, the Decoder takes sk 1 as its input

The sequence s(k) is generated in the Error Correction Signal Generator and plays a central role in the method. Generation of error correction Signal is according to the following rule: See definition of s(k) in example 3 and also drawing 5. Since binary information is represented by 0 and 2, **precoding** and decoding operations are given in terms of modulo-4 instead of modulo-2.

- The above table shows that c becomes 1 due to noise or intersymbol interference. The corresponding b(2) takes the value of 3 which is an illegitimate level. Therefore an error control signal s(2) is added to the decoder output a(2), yielding the corrected output a(2). The error correction signal [s(k)] is fed back with a unit **delay** so that the effect of and ambiguous level, 1 or -1, does not propagate in sequences [b(k)] and [a(k)].
- Example 2 m = 2, G(D) = 1-D, the same as in Example 1.
- Information sequence [a(k)], see the following table, is exactly the same as in Example 1. Hence, the first three rows of the table remain the same. However an ambiguous level reception now occurs at k = 1. Digital Demodulator output b is inside the range 0 </- b </- 2 and therefore the error correction signal cannot be generated instantly. As the sixth row of the table shows, the error correction signal is generated at k = 3 and can be used to correct a(1). Sequence [i(k)] of the eighth row is a sequence which stores the location of ambiguous level digits; i.e., i(k) = 1 if and only if c(k) = 1 or -1 and i = 0 otherwise.

See original p1727.

- As shown in examples 1 and 2, errors can be corrected either immediately or with some **delay**. If the maximum **delay** is d digits, one possible configuration of the error control circuit is given by drawing 3. Decoder output [a(k)] is passed into a storage d digit long. Since [a(k)] takes one value out of 2, 1 and 0, shift

registers of 2 bits can be used for the storage. Error-location indicator sequence [i(k)] is stored in a separate storage of the same length. The binary sequence [i(k)] operates as a gating signal to the error correction signal s(k), (k'(>/-k). The correction term sgn(s(k),) is added to a(k) if i(k) = 1, where sgn(x) is defined by
See original p1728. Single Error Correction.
- A single error is defined to be a digit x that falls in an ambiguous zone, i.e., c(k) = 1 or -1 in the present example, and is separated from adjacent errors by more than d digits. The probability that a single error can be corrected is
p/(s)/(c) = 1 - 2 over 3 . (1 over 2)d
Drawing 4 shows P/(s)/(c) vs. d.
- A single error can be corrected with probability 91.7, 97.9 and 99.94% with the storage length d=3, 5, and 10 digits, respectively.
Double Error Correction.
- Double errors are defined to be a pair of errors whose separation is less than d digits. The error correction circuit of drawing 3 can be applied to the case of double errors as shown in example 3.
- Example 3.m = 2, G(D) = 1 -D, magnetic **recording** with NRZI
See original p1728.
- In this example, errors occur at k = 1 and 2. Since both errors are of the same polarity, the error propagation pattern in the sequence [b(k)] add each other. Thus, illegitimate level -2 occurs at k = 3. The error correction signal [s(k)] is generated according to the following rule, drawing 5.
- Double errors with additive error propagation patterns are correctable. If the error propagation patterns have the opposite polarity, they cancel each other. These double errors are still correctable if the error control signal corresponding to the first error occurs before the second error takes place. Improvement of Error Correction by a **Parity** Check.
- The performance of the error correcting method discussed above depends on choice of the storage length d. The maximum **delay** d should not be too small. Otherwise, some of single errors remain uncorrected, drawing 4. However, the size of storage can be reduced by use of a **parity** check **code**.
See original p1729.
Then the **precoder** output b/1/(n) satisfies
b/1/(n) = 0 for all 1.
- This equation can be utilized directly for the purpose of error correction. The error correction signal s/1/(n) at the n-th digit of the l-th block is given by
s/(1)/(n) = -b/(1)/(n).
- The decoder structure is exactly the same as drawing 3 in which the maximum **delay** is now chosen equal to (n-1).
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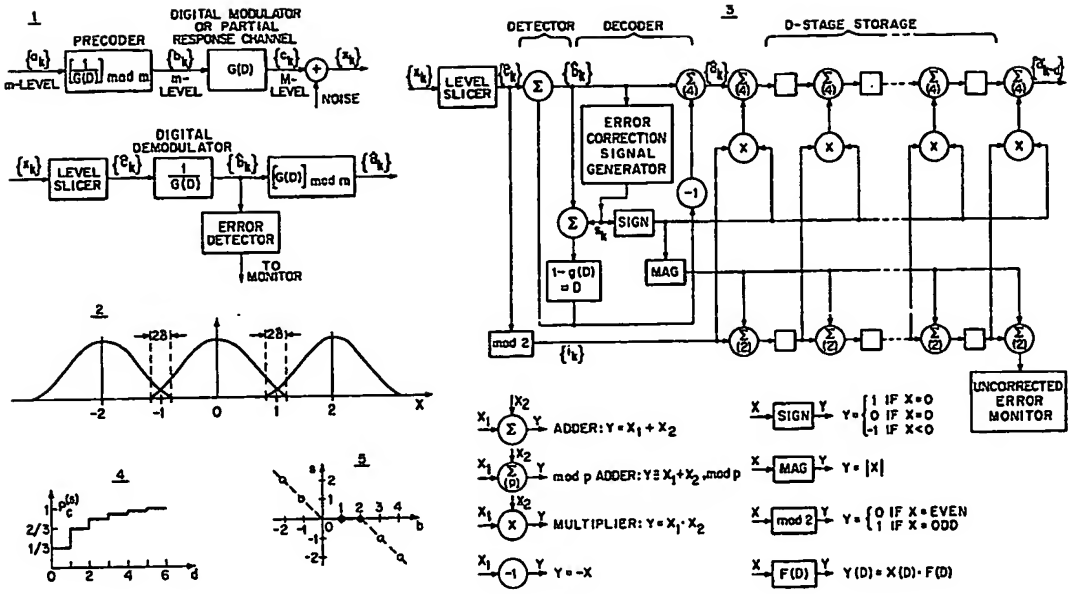

$$\hat{c}_k = \begin{cases} 2, & x_k > 1+\delta \\ 1, & |x_k - 1| < \delta \quad \text{: ambiguous zone} \\ 0, & |x_k| < 1-\delta \\ -1, & |x_k + 1| < \delta \quad \text{: ambiguous zone} \\ -2, & x_k < -1-\delta \end{cases}$$

k	0	1	2	3	4	5	
a_k	0	2	0	2	2	2	: Binary Sequence of 0 and 2.
$b_k = b_{k-1} \oplus a_k \pmod 4$	0	2	2	0	2	0	: Precoder Output (NRZI Output)
$c_k = b_k - b_{k-1}$	0	2	0	-2	2	-2	: Channel Output in the Absence of Noise
$\hat{c}_k$	0	2	(1)	-2	2	-2	: Level Slicer Output (An ambiguous level is circled.)
$\hat{b}_k = \hat{c}_k + (\hat{b}_{k-1} + s_{k-1})$	0	2	[3]	0	2	0	: Digital Demodulator Output.
s_k	0	0	-1	0	0	0	: Error Correction Signal.
$\hat{a}_k = \hat{b}_k \oplus (\hat{b}_{k-1} + s_{k-1}) \pmod 4$	0	2	1	2	2	2	: Decoder Output.
$a_k = \hat{a}_k \oplus s_k$	0	2	0	2	2	2	: Corrected Output.

$$s_k = \begin{cases} -1, & \text{for } b_k = 3 \\ 0, & \text{for } b_k = 2, 1, 0 \\ 1, & \text{for } b_k = -1 \end{cases}$$

k	0	1	2	3	4	5	
a_k	0	2	0	2	2	2	
$b_k = b_{k-1} \oplus a_k$	0	2	2	0	2	0	
$c_k = b_k - b_{k-1}$	0	2	0	-2	2	-2	
$\hat{c}_k$	0	(1)	0	-2	2	-2	
$\hat{b}_k = c_k + (\hat{b}_{k-1} + s_{k-1})$	0	1	1	[-1]	2	0	
s_k	0	0	0	1	0	0	
$\hat{a}_k = \hat{b}_k \oplus (\hat{b}_{k-1} + s_{k-1})$	0	1	0	2	2	2	
i_k	0	1	0	0	0	0	: Error-location Indicc Sequence.
						2	

$$\mathrm{sgn}(x) = \begin{cases} 1 & \text{for } x > 0 \\ 0 & \text{for } x = 0 \\ -1 & \text{for } x < 0 \end{cases}$$

$$P_c^{(s)} = 1 - \frac{2}{3} \cdot \left(\frac{1}{2}\right)^d$$

k	0	1	2	3	4	5	
a_k	0	2	0	2	2	2	: Binary Sequence of 0 and 2.
$b_k = b_{k-1} \oplus a_k \pmod 4$	0	2	2	0	2	0	: Precoder Output (NRZI Output)
$c_k = b_k - b_{k-1}$	0	2	0	-2	2	-2	: Channel Output in the Absence of Noise.
$\hat{c}_k$	0	(1)	(-1)	-2	2	-2	: Level Slicer Output.
$\hat{b}_k = c_k + (\hat{b}_{k-1} + s_{k-1})$	0	1	0	[-2]	2	0	: Digital Demodulator Output.
s_k	0	0	0	2	0	0	: Error Correction Signal.
$\hat{a}_k = \hat{b}_k \oplus (\hat{b}_{k-1} + s_{k-1}) \pmod 4$	0	1	3	2	2	2	: Decoder Output.
i_k	0	1	1	0	0	0	: Error-Location Indicator.
$a_k = \hat{a}_k \oplus i_k \cdot \mathrm{sgn}(s_{k'})$ $k \le k'$	0	2	0	2	2	2	: Corrected Sequence.

$$s_k = \begin{cases} -(\hat{b}_k - 2) & \text{for } b_k > 2 \\ 0 & \text{for } 0 \le b \\ -\hat{b}_k & \text{for } b_k < 0 \end{cases}$$

Let $\left\{a_k^{(\ell)}\right\} = \left\{ a_1^{(1)}, \ldots, a_n^{(1)}, a_1^{(2)}, \ldots, a_n^{(2)}, \ldots, a_1^{(\ell)}, \ldots, a_k^{(\ell)}, \ldots, a_n^{(\ell)}, \ldots \right\}$

k	1	2	3	4	5	6	
$a_k^{(\ell)}$	2	0	0	0	0	2	: Binary Sequence of the ℓ-th Block.
$b_k^{(\ell)} = b_{k-1}^{(\ell)} \oplus a_k^{(\ell)} \pmod 4$	2	2	2	2	2	0	: Precoder (NRZI) Output.
$c_k^{(\ell)} = b_k^{(\ell)} - b_{k-1}^{(\ell)}$	2	0	0	0	0	-2	: Channel Output in the Absence of Noise.
$\hat{c}_k^{(\ell)}$	2	(-1)	0	0	0	-2	: Level Slicer Output.
$\hat{b}_k^{(\ell)} = \hat{c}_k^{(\ell)} + (\hat{b}_{k-1}^{(\ell)} + s_{k-1}^{(\ell)})$	2	1	1	1	1	[-1]	: Digital Demodulator Output.
$s_k^{(\ell)}$	0	0	0	0	0	1	: Error Correction Signal.
$\hat{a}_k^{(\ell)} = \hat{b}_k^{(\ell)} \oplus (\hat{b}_{k-1}^{(\ell)} + s_{k-1}^{(\ell)})$	2	3	0	0	0	2	: Decoder Output.
$i_k^{(\ell)}$	0	1	0	0	0	0	: Error-Location Indicator.
$a_k^{(\ell)} = \hat{a}_k^{(\ell)} \oplus i_k^{(\ell)} \cdot \mathrm{sgn}(s_{k'}^{(\ell)})$ $k \le k'$	2	0	0	0	0	2	: Corrected Output.